Reduction of EMI Susceptibility in CMOS Bandgap Reference Circuits

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***Abstract*—This paper presents a successful approach to increase the electromagnetic interference (EMI) immunity of CMOS bandgap reference circuits. Layout techniques along with some changes in the reference schematics lead to a robust electromagnetic immunity, preserving good overall performances. Measurement results confirm the low susceptibility of the proposed circuits. They exhibit only a few millivolts shift, for interfering signals of 1 Vpp in the frequency range of 1 MHz to 4 GHz, compared to the classical topologies that may reach more than 1 V. The circuits were fabricated in a 0.8-μm standard CMOS technology.**

***Index Terms*—CMOS bandgap voltage reference, immunity to electromagnetic interferences, operational amplifier, symmetric topology.**

I. Introduction

In recent years, due to the increasing adoption of electronic and microelectronic equipment, the immunity to electromagnetic interference (EMI) is becoming an important issue for integrated circuit (IC) designers. Indeed, EMIs may potentially affect any kind of circuit and may arise from a wide class of sources (cellular phones, CD players, laptop computers, etc.).

Furthermore, due to a high density of components packed on printed circuit boards (PCBs), as well as due to the increasing speed of the mixed analog/digital circuits, IC designers have to consider EMI during the design phase. Neglecting these aspects may lead to failures in ICs induced by spurious signals, also including frequencies outside the operating bandwidth of the circuit [1], [2].

The lack of EMI immunity forces IC designers to reduce the circuit susceptibility by means of *a posteriori* PCB layout adjustments, filters, change in the operating frequency, shielding, etc., which are complex, expensive, and seldom viable.

Therefore, in recent years, EMI effects were carefully investigated both theoretically and experimentally in order to find possible prevention methodologies, in particular, in analog ICs, which include operational amplifiers [3], [4]. It is worth adding that many other analog circuits may be affected by EMI. Among them, the bandgap voltage reference is a very critical one, because it is adopted in many modern very large scale integration (VLSI) applications. For example, the resolution of the integrated data acquisition circuits such as analog-to-digital or digital-to-analog converters is ultimately limited by the precision of the reference voltages.

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In the literature, much attention is paid to many quality aspects, such as the mean relative temperature dependency, accuracy, etc., but the influence of EMI is generally not treated explicitly or even neglected.

It is worth adding that among various voltage reference architectures, the most popular circuit is the bandgap reference based on p–n junctions, OpAmp, and resistors [6]. On the other hand, in order to meet the important constraints of low power supply voltage and low power dissipation, it is desirable to use simple architectures, avoiding operational amplifiers and additional circuits. Therefore, many different bandgap architectures were also designed [7].

This paper describes an approach to improve the immunity to EMI of CMOS bandgap references. In particular, two architectures have been investigated: The first one is a bandgap circuit based on the ratioed resistors and OpAmp; the second one uses the ratioed transistors biased in strong inversion along with the inverse-function technique to produce temperature-insensitive voltage references. In Section II, the effects of EMI are discussed; in Section III, the design of high-immunity bandgap references is presented; and in Section IV, measurement results are provided and discussed.

II. EMI Effects in Voltage Reference Circuits

In order to reach a clear comprehension of the EMI on a bandgap reference circuit, it should be pointed out that in many applications, analog and digital subsystems are required to coexist on the same chip, sharing the same power sources. In such a system, EMI may arise from external circuits as well as from subsystems integrated on the same die, spreading through the supply lines leading to large unexpected fluctuations of the power supply.

In order to investigate EMI effects on the bandgap references, interference is modeled by means of spurious signals applied to the power pins. In [2], EMI is often represented by means of undamped sinusoidal waveforms that allow for easy measurement in the laboratory. The amplitude of the interfering sinusoidal signal is assumed 1 Vpp (which is a large value if compared to the 3.3-V voltage supply), with 0 dc mean value, and the frequency ranging from 1 MHz to 4 GHz, accounting for a wide range of interfering signals.

Simulations and measurements on analog circuits show that the most undesirable effect of interference is a large shift of the dc mean voltages. In particular, the EMI susceptibility may be easily correlated to some specific features of the OpAmp transient responses [2]–[4]. Simulations and measurements were performed on different architectures—Miller OpAmp, Cascode,

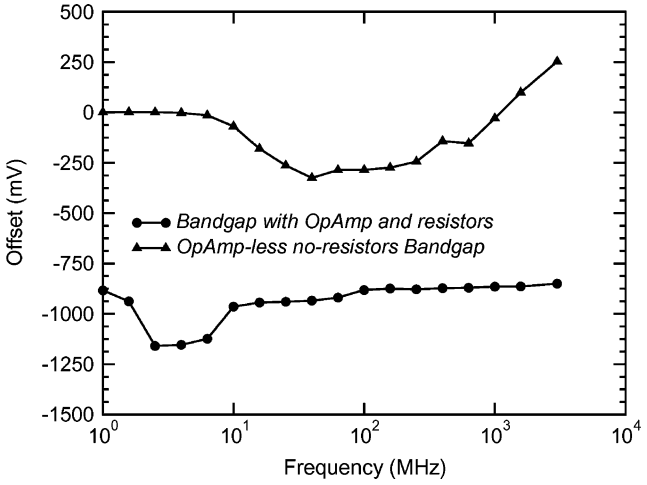

Fig. 1. Effect of EMI (1 Vpp) conveyed on Vdd. Offset of the reference voltage $V_{\rm ref}$ for a bandgap based on OpAmp and resistors [5] and for a bandgap without OpAmp [6].

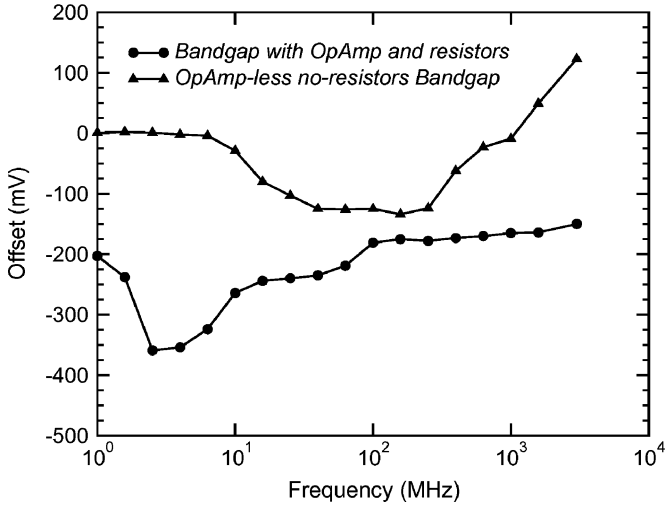

Fig. 2. Effect of EMI (100 mVpp) conveyed on Vdd. Offset of the reference voltage $V_{\rm ref}$ for a bandgap based on OpAmp and resistors [5] and for a bandgap without OpAmp [6].

Folded Cascode OpAmp, and so on—comparing single-ended and fully differential amplifiers. They have emphasized a correlation between EMI-induced dc output and asymmetric slew rates. In particular, if the magnitude of the positive slew rate is larger than the negative one, rising transients are faster than the falling ones, and the output voltage usually exhibits a positive shift of the dc mean value. Furthermore, the parasitic capacitances play a significant role in determining the out-of-band OpAmp behavior.

With regard to the bandgap circuits, the effect of EMI applied to the power pin may induce serious failures, and the voltage reference may, indeed, reach a shift of many hundreds of millivolts. The results of simulations performed on two different bandgap circuits are plotted in Fig. 1: The first is a bandgap circuit based on OpAmp and resistors [6], and the second does includes neither OpAmps nor resistors [7].

As shown in the figure, the offset of a classical topology-based on amplifier and resistors may reach more than 1 V, while the maximum offset of a bandgap without OpAmp reference is of about 350 mV; both are unacceptable for many applications.

In Fig. 2, similar simulations are carried out with a power line noise of 100 mVpp. The offset of the bandgap reference circuits is still very large. It is worth noting that filtering the supply lines on chip is seldom viable and often expensive. It leads to a large area consumption, and in order to account for the distributed nature of the supply ring, the filtering should spread all around the chip.

III. Design of High-Immunity Bandgap Reference Circuit

A. First Bandgap: Based on OpAmp and Resistors

The architecture of such a bandgap is shown in Fig. 3. The large offset seen in Fig. 1 arises from the amplifier stage and from the large fluctuations of $V_{\rm ref}$. The latter creates voltage oscillations on the OpAmp input nodes; hence, by minimizing these oscillations and the EMI susceptibility of the OpAmp,

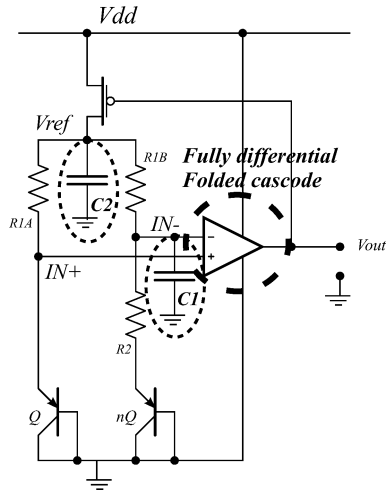

Fig. 3. Final bandgap circuit.

the bandgap EMI immunity is strongly improved. A promising approach to reducing the susceptibility of the OpAmps is proposed in [3] and [4], and the corresponding schematic is shown in Fig. 4. It is based on a fully differential folded cascode architecture whose main features are large gain, which is important for the correct behavior of the overall bandgap circuit, good rejection of the common mode signals (CMRR), and high power supply rejection ratio (PSRR), thanks to the folded cascode connection [5], and symmetric slew rates, which play a significant role in terms of EMI immunity. Furthermore, the amplifier stage is simple and does not require a remarkable area consumption.

Thanks to the symmetry of the amplifier stage, the immunity level of the bandgap in Fig. 3 is enhanced by more than one order of magnitude. In particular, the offset of the reference voltage is low (few tens of millivolts) at low-medium frequencies, while at larger frequencies (up to 60 MHz), the bandgap exhibits an offset of about 200 mV. Similar considerations hold when the interfering signal is applied to the ground pin.

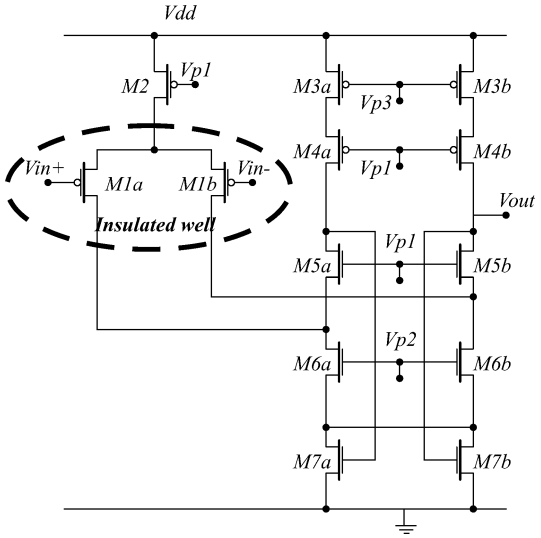

Fig. 4. Schematic of a high EMI immunity OpAmp topology.

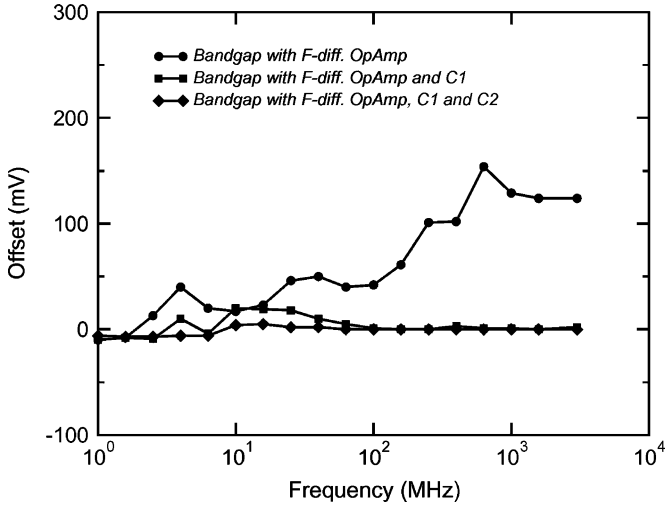

Fig. 6. Offset of the improved bandgap based on OpAmp and resistors.

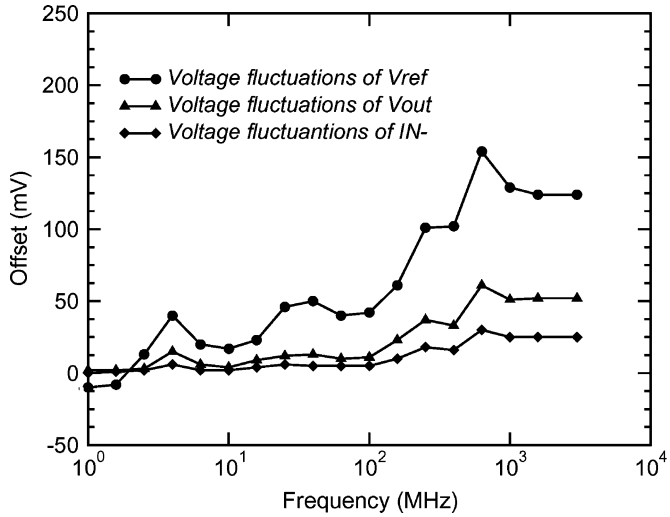

Fig. 5. Voltage offset at $V_{\rm ref}$, $V_{\rm out}$, and IN–.

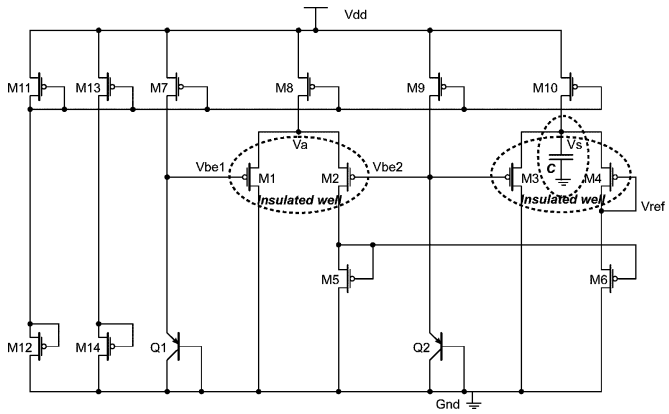

Fig. 7. Second bandgap with improved EMI immunity.

When EMI immunity is addressed, layout issues are as important as circuit considerations. Therefore, two different layout designs were extracted and simulated. In the first one, the differential pair of the OpAmp was created in a common n-well (the bulk terminal is connected to Vdd); in the second, the differential pair was created in an insulated well with the bulk terminal connected to the common source. The insulated well is, therefore, simulated as a large diode in inverse polarization; its size is computed by the circuit extractor. The second design exhibits a reduced susceptibility, because the interfering signals, coming from the power supply, are not directly connected to the bulk terminal of the differential pairs. As expected, simulation results show that the amplifier using an insulated well for the P-MOS differential pair exhibits a slightly reduced offset (of about 25%). It reaches 150 mV instead of 200 mV at high frequencies. A possible solution to further reduce the voltage fluctuations plotted in Fig. 5 on the most critical nodes of the circuit of Fig. 4 is placing two small capacitors (1 pF) between the negative input of the OpAmp (IN–) and ground as well as between the reference voltage node (Vref) and ground. Simulations performed on the final circuit are reported in Fig. 6.

It is worth noting that the capacitors C1 and C2 do not influence the standard behavior of the bandgap reference. Along with a good EMI immunity, the voltage reference retains good overall performances, in terms of the temperature coefficient (0.032 mV/°C) and power consumption (0.84 mW).

B. Second Bandgap: Bandgap Without OpAmp

The schematic of the bandgap reference circuit is detailed in [8] and shown in Fig. 7. With regard to this bandgap topology, analysis and simulations emphasized that the differential pairs (M1–M2 and M3–M4) play a significant role on the EMI susceptibility. Hence, in order to improve the immunity to interference, M1–M2 and M3–M4 are created in insulated wells, and a small capacitor (1 pF) is connected between Vs and ground, using the promising approach discussed in [8] and detailed in the previous subsection. In Fig. 8, the results of the circuit simulations are reported.

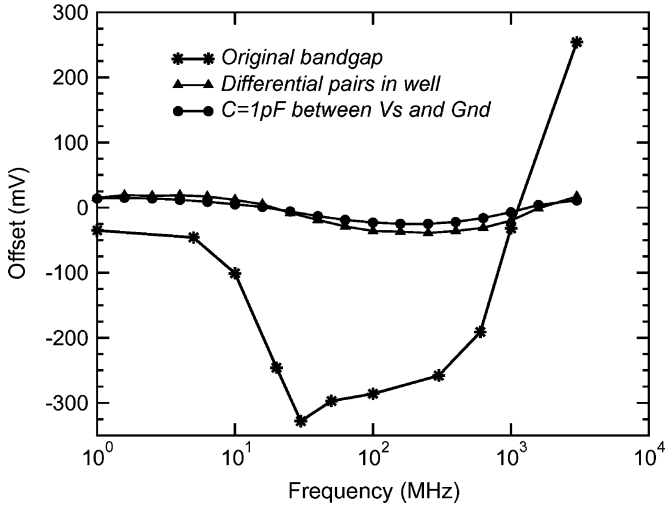

Fig. 8. Offset of the improved bandgap without OpAmp.

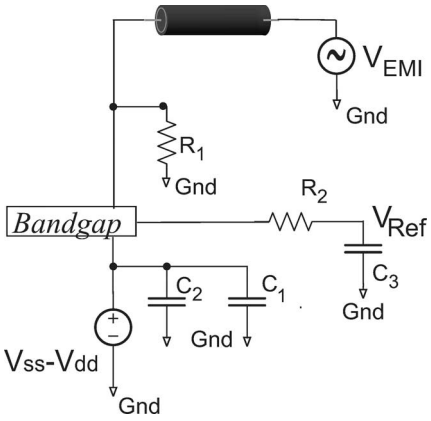

Fig. 9. Circuit for EMI measurements in the case of EMI applied to the Vdd pin. The boxed area "Bandgap" means bandgap under test and refers to both the bandgap topologies.

It is worth adding that the small capacitor C does not significantly influence the behavior of the bandgap references. Furthermore, along with a good EMI immunity, the voltage reference retains good overall performances: The temperature coefficient TC is 0.010 mV/°C and the power consumption is about 1.7 mW.

IV. Measurements and Result

A. Measurements Setup

In order to investigate the EMI immunity level, the interfering signals were modeled by means of the sinusoidal waveforms applied to the power pins by means of a coaxial cable terminated by a 50-Ω equivalent resistor. The amplitude of the interfering signal was assumed to be 1 Vpp, with 0-dc mean value [2]. The frequency ranges from 1 MHz up to 4 GHz, in order to account for the spectrum of many of the possible interfering signals including the cellular phone bands.

With regard to the EMI measurement setup, shown in Fig. 9, we designed the board interconnections as short as possible, along with straight paths and ground shields, in order to minimize the undesired signals arising from the measurement setup itself. Two capacitors ($\mathrm{C1} = 100$ nF and $\mathrm{C2} = 10\,\mu$F) are used to stabilize the Gnd line when the interfering signals are applied to Vdd and a resistor ($\mathrm{R1} = 50\,\Omega$) is used to fulfill the instrumentation load requirements, i.e., for the impedance matching. Furthermore, the output is connected to an $RC(\mathrm{R2} = 1\,\mathrm{k}\Omega, \mathrm{C3} = 1\,\mathrm{nF})$ filter with a cutoff frequency of 160 kHz in order to extract the output mean voltage, which is strictly correlated to the dc shift arising from the EMI. It is worth noting that the RC filter does not significantly influence the overall bandgap behavior.

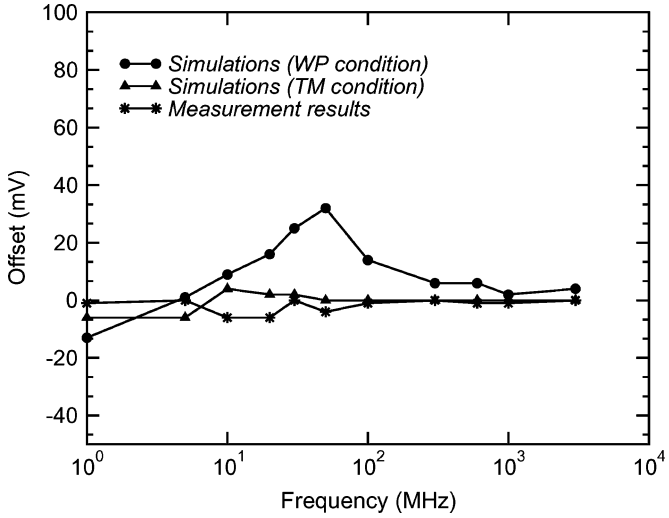

Fig. 10. Offset of the first bandgap. Measurement and simulation results for interfering signals of 1 Vpp.

Finally, the measurement board was shielded with an RF metal box in order to minimize the interferences arising from the environment. Measurements performed using a vector network analyzer (VNA) show that the adopted RF metal box exhibits an almost ideal behavior, providing an attenuation of 70–80 dB in the whole measured frequency range.

B. Measurement Results

1) Bandgap Based on OpAmp and Resistors: The experimental results are shown in Fig. 10, for the case of interfering signals applied to Vdd with 1 Vpp. The offset of the proposed bandgap is very low: Its maximum value is about 6 mV in the whole frequency range, which is more than two orders of magnitude smaller than the bandgap based on single-ended OpAmps. Similar results are obtained when the interfering signal is applied to the ground. In this figure, the experimental results are also compared to the simulated ones under typical mean and worst-case power conditions. As depicted in Fig. 11, four different worst-case models are available for the CMOS process in the simulator Spectre: the worst-case power condition WP (both P- and N-MOS are faster than the mean condition TM), the worst-case speed condition WS (both P- and N-Mos are slow), the worst-case one condition WO (P-MOS are slow while N-MOS are fast), and the worst-case zero condition WZ (P-MOS are fast while N-MOS are slow).

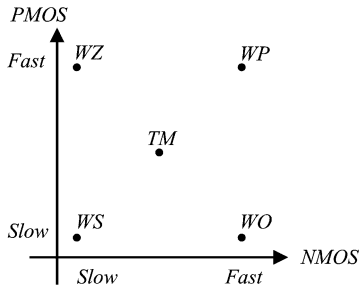

Fig. 11. Worst-case conditions.

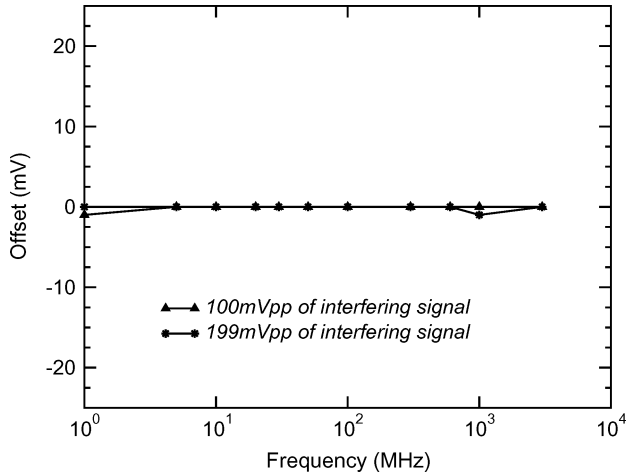

Fig. 12. Offset of the first bandgap. Measurement results.

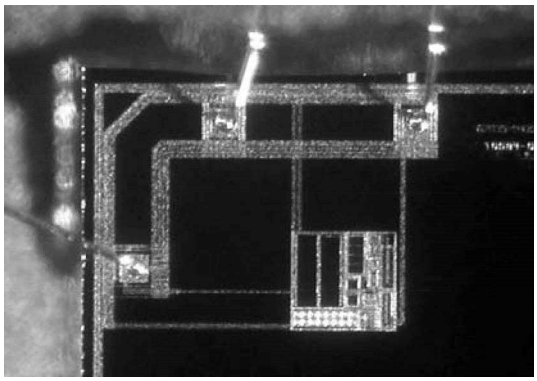

Fig. 13. Microphotograph of the first bandgap reference circuit.

Measurements were also performed with interfering signals of 100 and 199 mVpp, which represent typical power line noises, as in the Electromagnetic Compatibility Standard EN-61000, and the experimental results are shown in Fig. 12. Fig. 13 shows a snapshot of the circuit fabricated in the 0.8-μm AMS CMOS CXQ technology. The minimum fabrication area was 10 mm^2, while the bandgap area is only 0.13 mm^2.

2) Bandgap Without OpAmp: The measured and simulated offset of the second bandgap are compared in Fig. 14. The maximum measured offset is about 60 mV at 300 MHz, which is nearly the same as the offset simulated in the worst-case power condition. However, at frequencies lower and higher than 300 MHz, the offset is smaller and more similar to that simulated in the typical mean conditions.

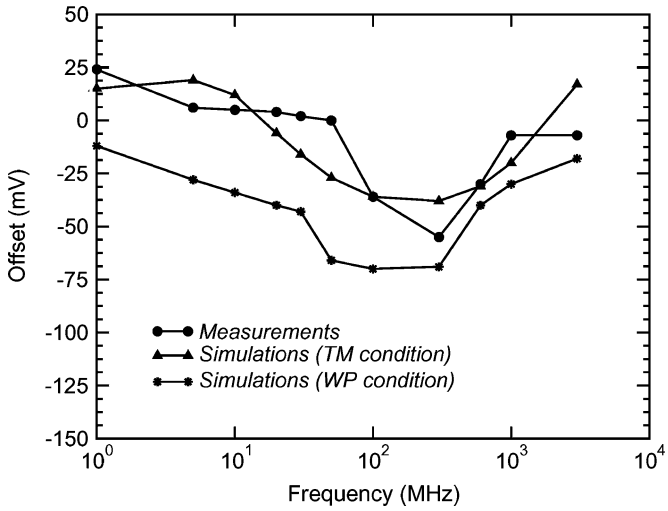

Fig. 14. Offset of the second bandgap. Measurement and simulation results.

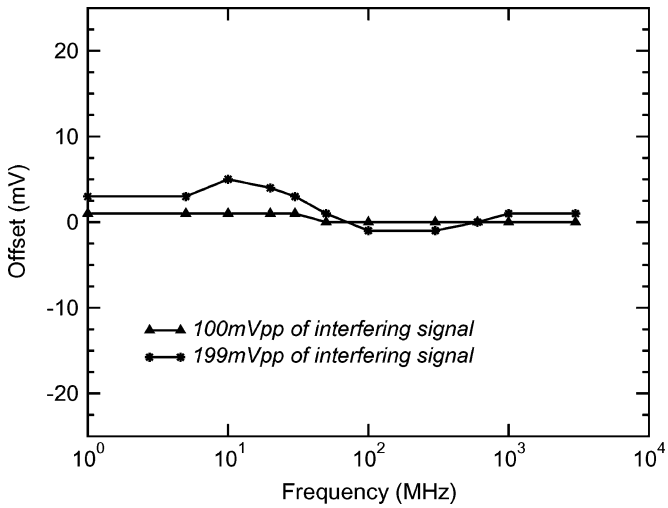

Fig. 15. Offset of the first bandgap. Measurement results.

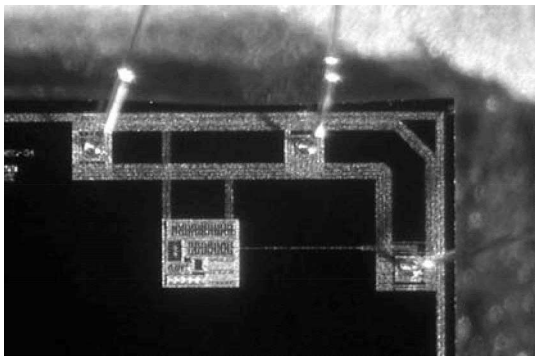

Fig. 16. Microphotograph of the second bandgap reference circuit.

In order to further test its robustness to interferences, measurements were performed with interfering signals of 100 and 199 mVpp, which represent typical power line noises. In Fig. 15, the experimental results are shown: As expected, the proposed bandgap exhibits a negligible offset. Fig. 16 shows the snapshot of the circuit fabricated in the 0.8-μm AMS CMOS CXQ technology.

V. Conclusion

In recent years, due to the increasing adoption of electronic equipment, the immunity to EMIs has become an important constraint for IC designers. EMI effects were carefully investigated in order to find possible prevention methodologies, in particular, for analog circuits.

This paper addresses the design of the bandgap reference circuits, which provide a good tradeoff between voltage reference performance and strong immunity to EMI, thanks to small changes in circuit schematics and layout techniques. Measurements are provided and compared to the simulations performed on the circuit extracted from the layout.

Acknowledgment

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